H/W Instruction Guide

- Model ： BP-FB1U04-TY
- P/N ： BBP-FB10007AA01
- Revision: A03

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EE1
2025.09.25
MK Sun

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Tables

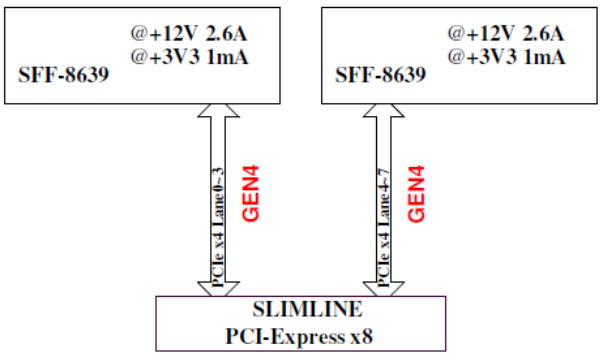
1. HISTORY

Revision	Date	Description of Changes
A01	2025-09-25	Preliminary release
A02	2022-04-12	(Page 9) SW502 : PCA9545 Address change to PCA9543 Address (Page 9) JSL_I2C1 settingUBM/VPP/SHP (default) change to UBM0 mode (default) (Page 9) JSL_I2C2 settingBMC change to Asrock MB mode
A03	2025-09-25	(Page 9) Added an Application Setting (Page 12) Add SOV table

2. HARDWARE OVERVIEW

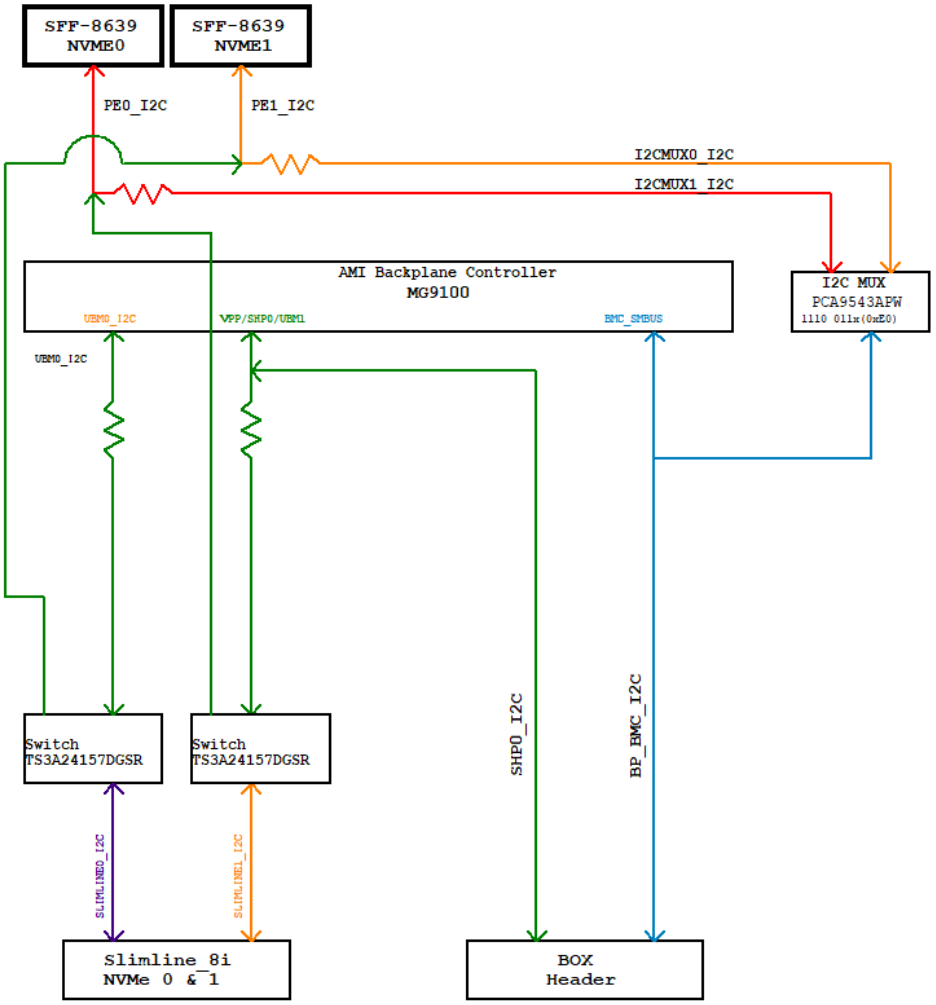
2.1 HW Block Diagram

Figure 1



2.2 SMBus Block Diagram

Figure 2

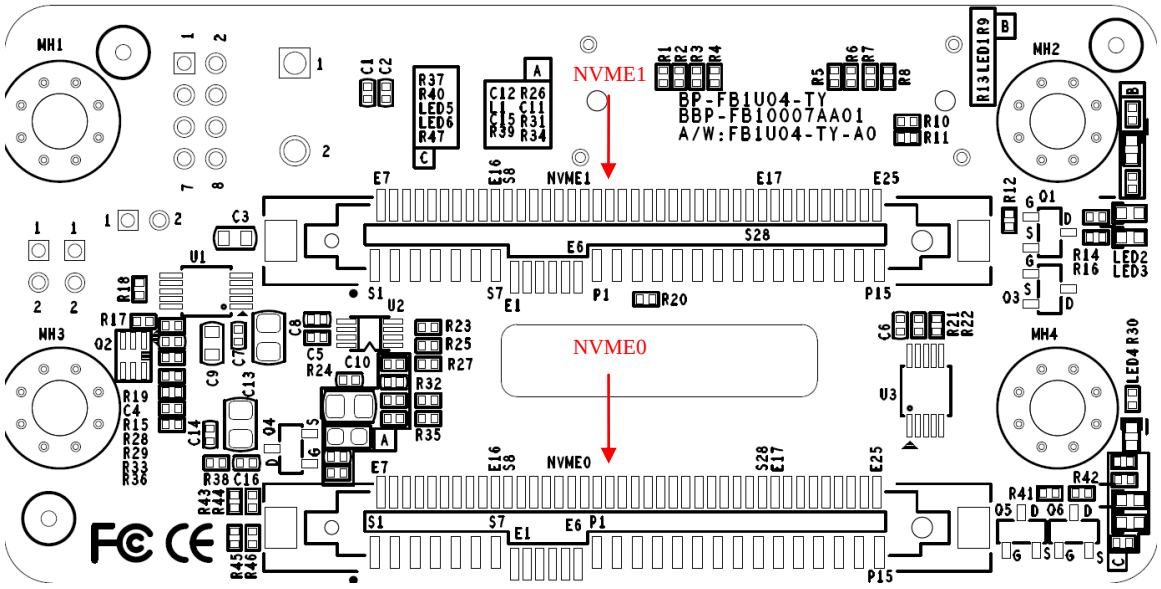


3. HARDWARE DESIGN SPECIFICATION

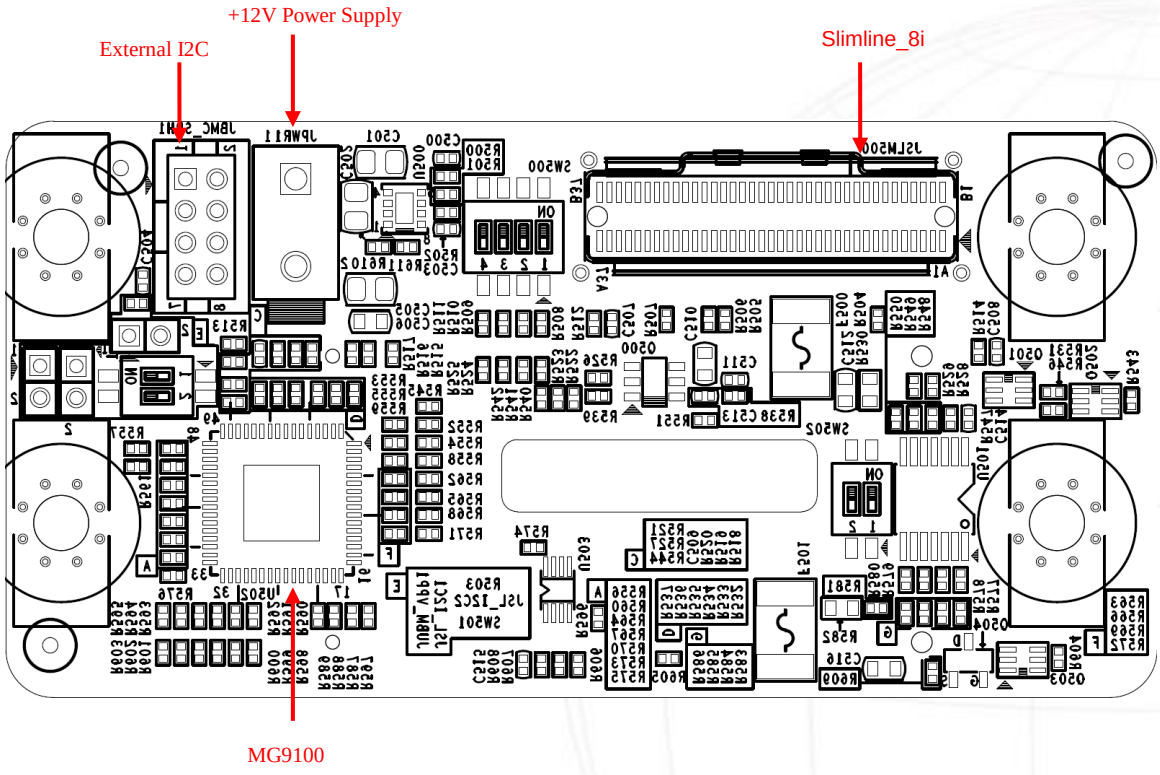
3.1 Placement

Figure 3
PCBA Placement

TOP



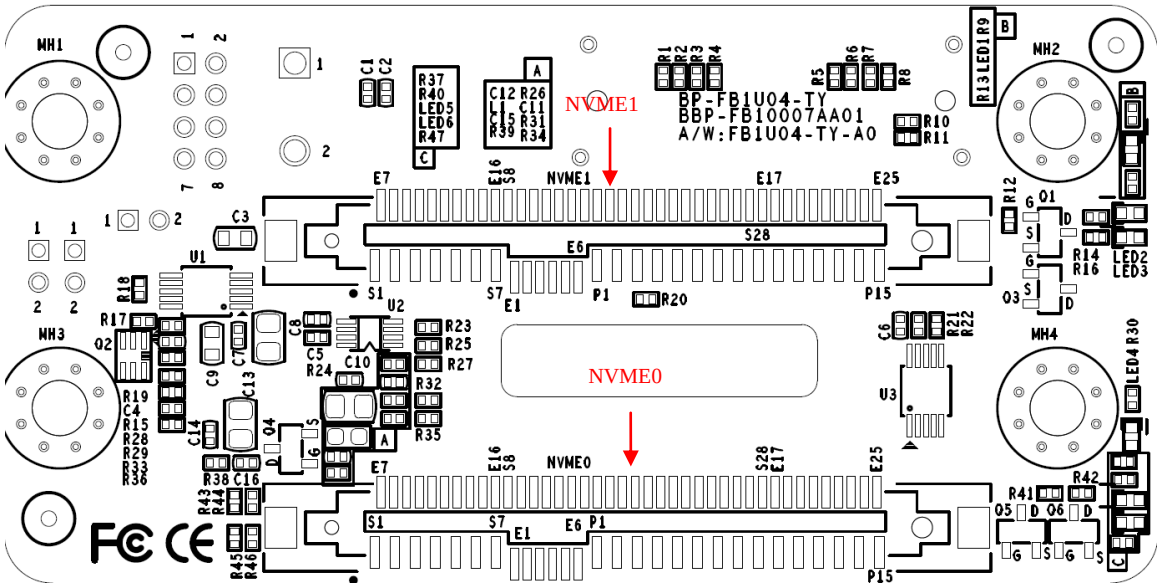
Bottom



3.2 Connector

Figure 4
Connector Location

TOP



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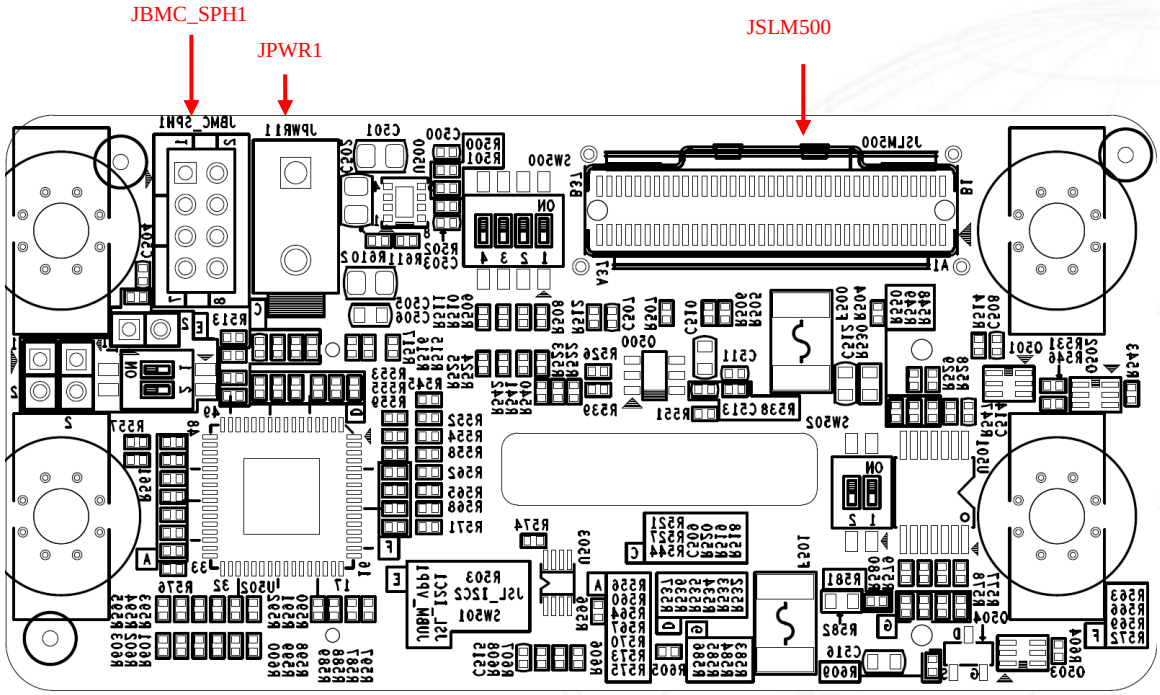


3.2.1 *External Connectors*

Table 1 External Connectors

Connector Function	Physical Description	Comments
NVMe SSD (NVME0,NVME1)	SFF-8639 NVMe Receptacle	NVMe SSD Connector
Slimline (JSLM500)	SFF-8654 Slimline	PCIeX4 Gen4

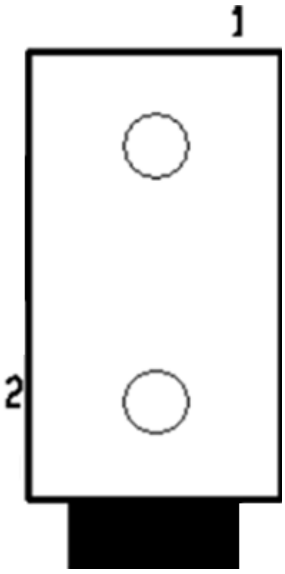
3.2.2 *Internal Connectors*

Table 2 Internal connectors Summary

Connector Function	Physical Description	Comments
Power Supply (JPWR1)	1x2 Power Connector ,PH5.5	+12V Power in, 8A per pin.
External I2C (JBMC_SPH1)	2x4 pin Box Header, PH1.25	I2C Input to MG9100– BMC /UBM0 / VPP0 I2C

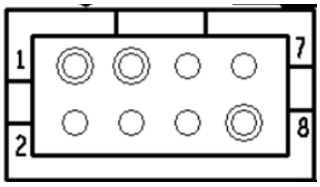
3.2.3 *Connector Pin-Out*

Power Supply – JPWR1



Pin	Description
1	GND
2	+12V

I2C Connector –JBMC_SPH1



Pin	Description	Pin	Description
2	BP_BMC_SCL	1	SHP0_SCL
4	BP_BMC_SDA	3	SHP0_SDA
6	GND	5	GND
8	BMC_SMBALRT_N	7	SHPINT_N0

3.3 LEDs

Figure 5 LED Location

TOP

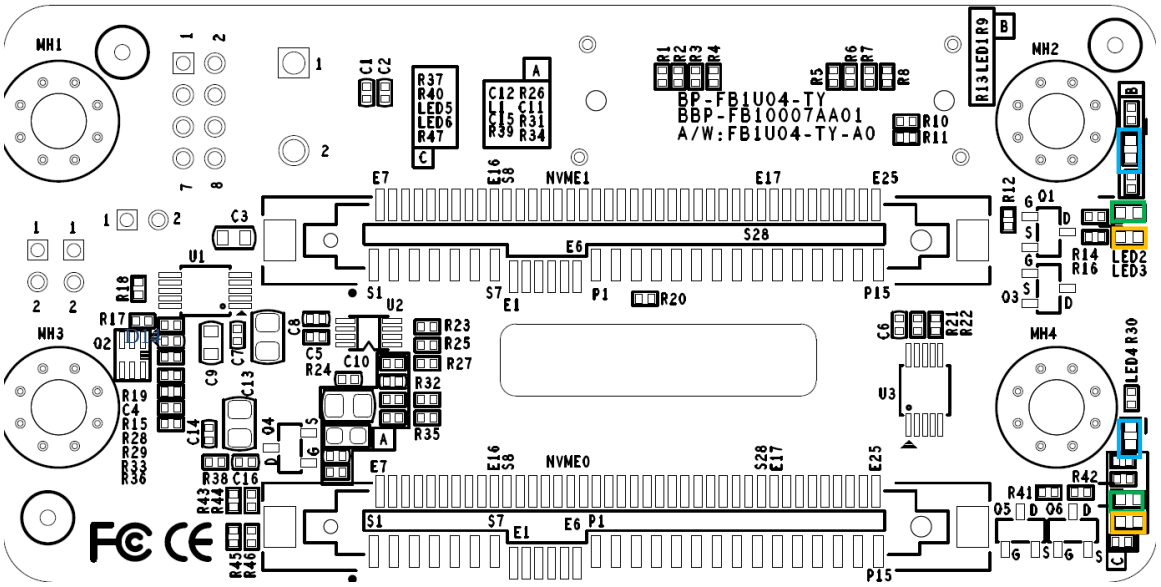
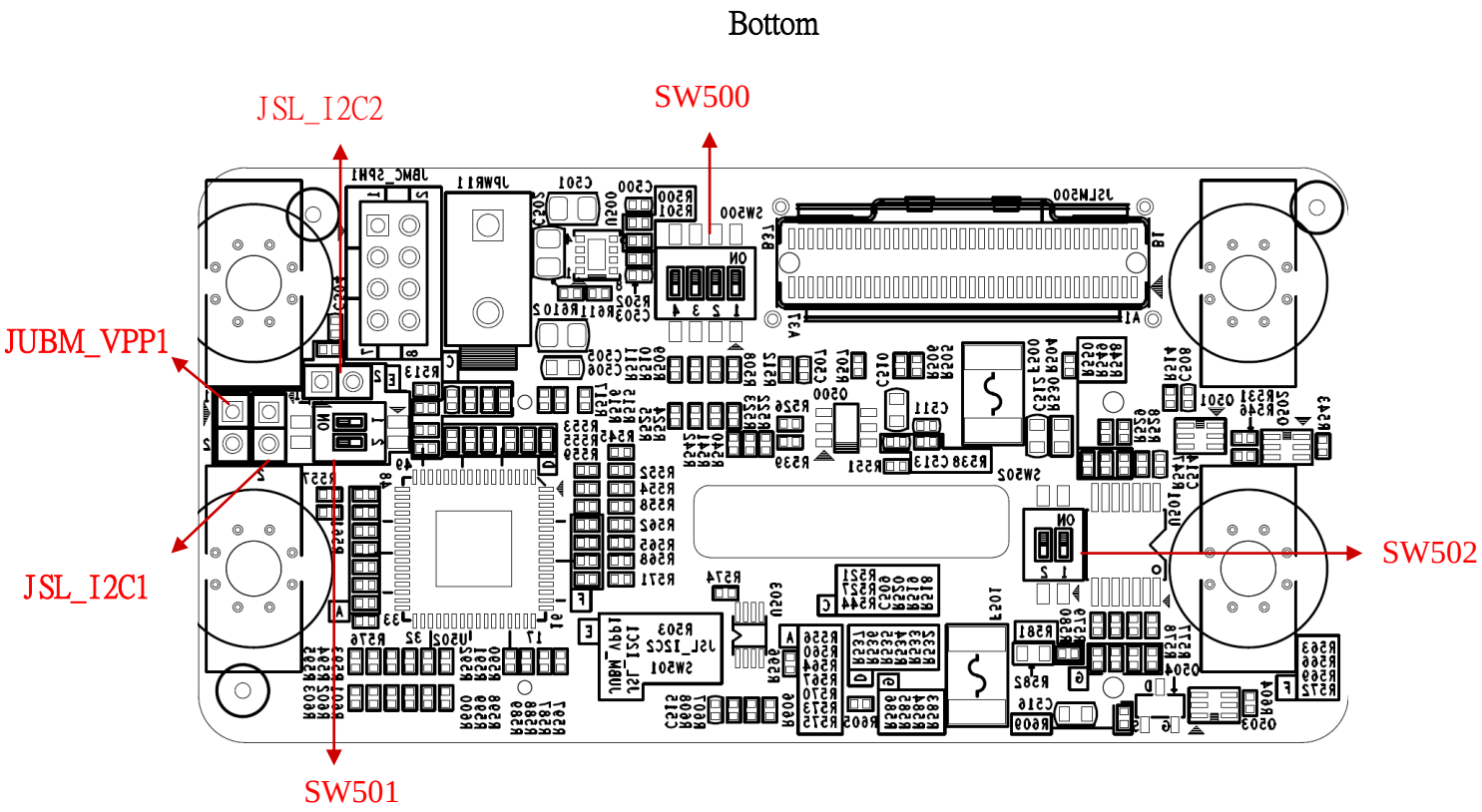


Table 3 LED Definition

HDD Activity LEDs(LED1,LED4)	Blue (On)	NVMe SSD present
	Blue (Blinking)	NVMe SSD Activity detected or External control
	Off	NVMe SSD not connect
HDD Attention LEDs(LED3,LED6)	Off	Normal
	YEL (On or Blinking)	External input Or NVMe SSD +12V Power OFF
HDD OEM LEDs(LED2,LED5)	Off	Normal
	GEN (On or Blinking)	OEM Command By External Input

3.4 DIP-Switch

Figure 6 DIP-Switch Location



3.4.1 *DIP-Switch Definition*

SW500

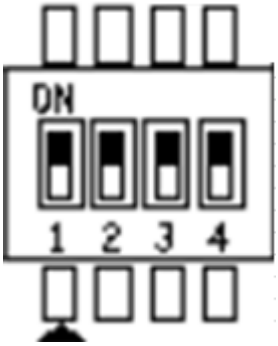
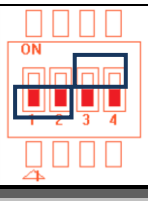


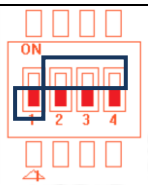
Table 4 –INTEL VPP ID configuration settings (Default)

(1) Support 8 address setting 0X40h/0X42h/0X44h/0X46h/0X48h/0X4Ah/0X4Ch/0X4Eh

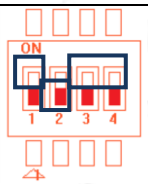
SW500 (Address: 0X40h / 0X42h)

8	7	6	5	
		ON	ON	
OFF	OFF			
1	2	3	4	

SW500 (Address: 0X44h / 0X46h)

8	7	6	5	
	ON	ON	ON	
OFF				
1	2	3	4	

SW500 (Address: 0X48h / 0X4Ah)

8	7	6	5	
ON		ON	ON	
	OFF			
1	2	3	4	

SW500 (Address: 0X4Ch / 0X4Eh)

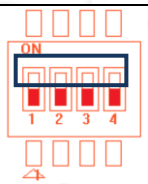
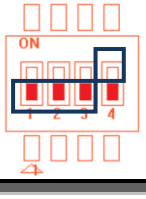
8	7	6	5	
ON	ON	ON	ON	
1	2	3	4	

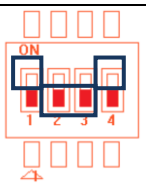
Table 5 –AMD SHP ID configuration settings

(1) Support 8 address setting 0X50h/0X52h/0X54h/0X56h/0X58h/0X5Ah/0X5Ch/0X5Eh

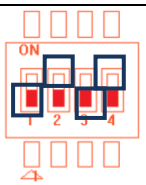
SW500 (Address: 0X50h / 0X52h)

8	7	6	5	
			ON	
OFF	OFF	OFF		
1	2	3	4	

SW500 (Address: 0X54h / 0X56h)

8	7	6	5	
ON			ON	
	OFF	OFF		
1	2	3	4	

SW500 (Address: 0X58h / 0X5Ah)

8	7	6	5	
	ON		ON	
OFF		OFF		
1	2	3	4	

SW500 (Address: 0X5Ch / 0X5Eh)

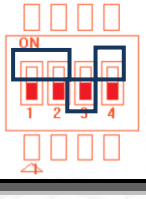
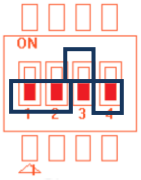
8	7	6	5	
ON	ON		ON	
		OFF		
1	2	3	4	

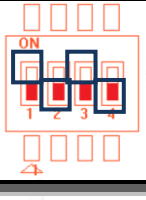
Table 6 –AVAGO SHP ID configuration settings

(1) Support 8 address setting 0X40h/0X42h/0X50h/0X52h/0X60h/0X62h/0X70h/0X72h

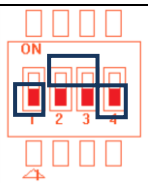
SW500 (Address: 0X40h / 0X42h)

8	7	6	5	
		ON		
OFF	OFF		OFF	
1	2	3	4	

SW500 (Address: 0X50h / 0X52h)

8	7	6	5	
ON		ON		
	OFF		OFF	
1	2	3	4	

SW500 (Address: 0X60h / 0X62h)

8	7	6	5	
	ON	ON		
OFF			OFF	
1	2	3	4	

SW500 (Address: 0X70h / 0X72h)

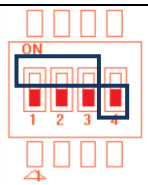
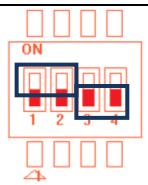
8	7	6	5	
ON	ON	ON		
			OFF	
1	2	3	4	

Table 7 –UBM ONLY SW500

8	7	6	5	
ON	ON			
		OFF	OFF	
1	2	3	4	

SW501

PIN1	PIN2	BMC Address
off	off	0xC6h
on	off	0xC4h
off	on	0xC2h
on	on	0xC0h(default)

SW502

PIN1	PIN2	PCA9543 Address
off	off	0xE6h
on	off	0xE4h
off	on	0xE2h
on	on	0xE0h(default)

JSL_I2C1

OPEN	Asrock MB mode
SHORT	UBM0 mode (default)

JSL_I2C2

OPEN	Asrock MB mode
SHORT	UBM1/SHP0 mode (default)

JUBM_VPP1

OPEN	VPP Operation(default)
SHORT	UBM Operation

4. STATEMENT OF VOLATILITY (SOV)

AIC products contain both volatile and non-volatile (NV) components. Volatile components lose their data immediately after power is removed from the component. Non-volatile (NV) components continue to retain their data even after power is removed from the component. This table describes the volatile and non-volatile storage components.

Table 8

Programmable Devices

Quantity	Reference	Description	Volatile	Manuf1_name	Manuf1_PN	AIC PN1_12	AIC PN15	User Accessible	Sanitization Procedure
1	U502	BP Management controller	No	AMI	MG9100_004m00	CM5-00006510	MP-00006510-000	No	None